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COSIC

The need for hardware roots of trust

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erc

Šibenik June 21, 2019

Slides credit: Miloš Grujić, Jeroen Delvaux, Kent Chuang, Adriaan Peetermans, Roel Maes and other PhD students

Outline

- Implementation Challenges
- Hardware roots of trust
- PUFs
- TRNG
- Conclusions

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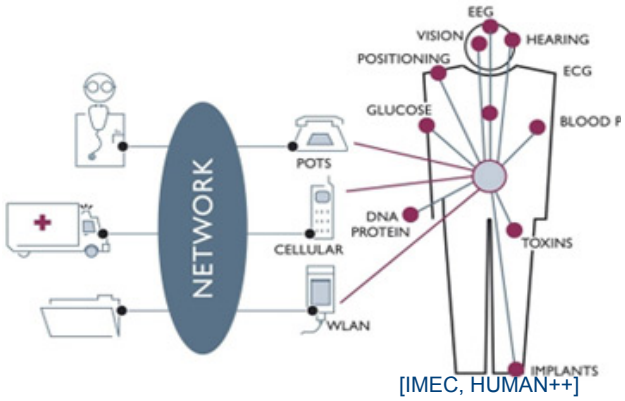
Internet of Everything – IOT – Industry4.0 E-…

- Internet of things
- E-health, e-commerce
- E-voting, e-…
- Smart grid
- Big data



[IMEC, HUMAN++]

Anything E- or Smart needs security

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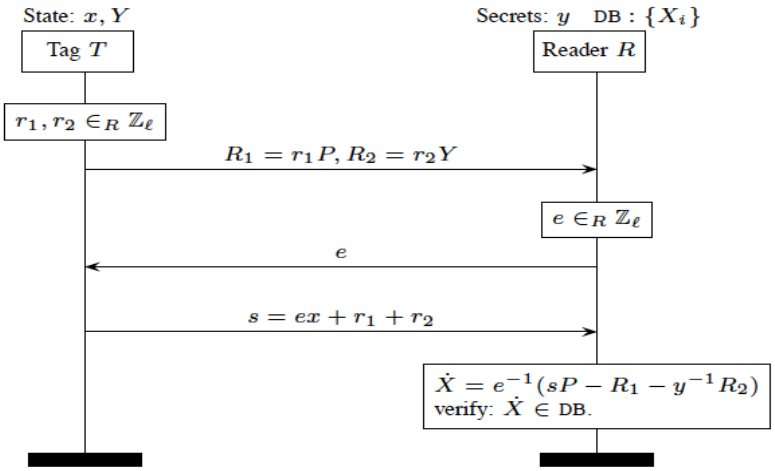
How the crypto protocol paper sees it:

Some calculations are **on** the arrows?



Source: J.Hermans, et al., "Proper RFID Privacy: Model and Protocols," IEEE Trans on Mobile computing, 2014

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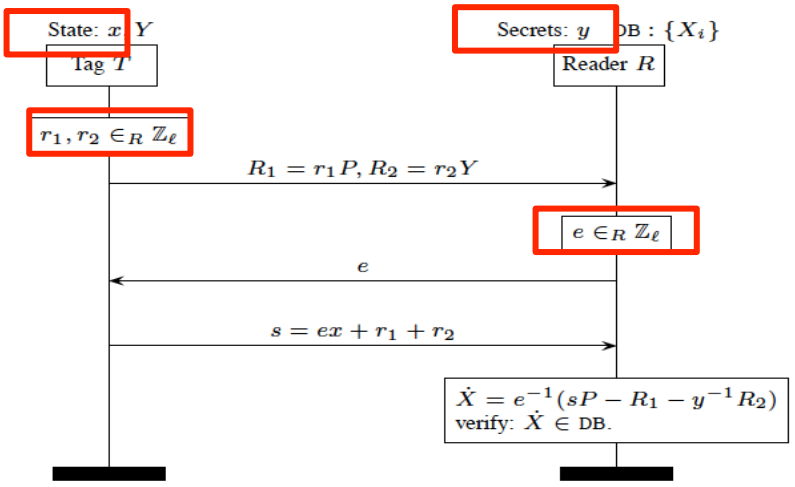
Protocol relies on secrets and random numbers



Source: J.Hermans, et al., "Proper RFID Privacy: Model and Protocols," IEEE Trans on Mobile computing, 2014

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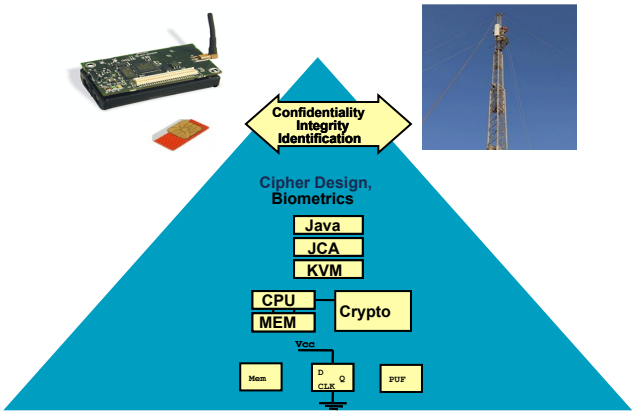
Root of Trust

DESIGN METHODS: DECOMPOSE IN COMPONENTS



- Application: secure communication
- Algorithms: public key, secret key, relies on secret key, post-quantum
- Architecture: Hardware/Software platform, Sancus
- Micro-architecture: crypto co-processors, instruction set extension,
- Logic circuits and (secure) memory
- TRNGs and PUFs

[DATE2007]

*"A root of trust is a component at a **lower** abstraction layer, upon which the system relies for its security."*

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How to store a secret?

Permanently: e.g. for a master key

- Fuses: large, visible, limited numbers
- Non-volatile memory: extra processing
- Battery-backed SRAM, cumbersome, battery can die
- PUFs: physically unclonable functions

= a cost-efficient replacement technology for secure non-volatile memory (NVM)

[PhD Jeroen Delvaux]

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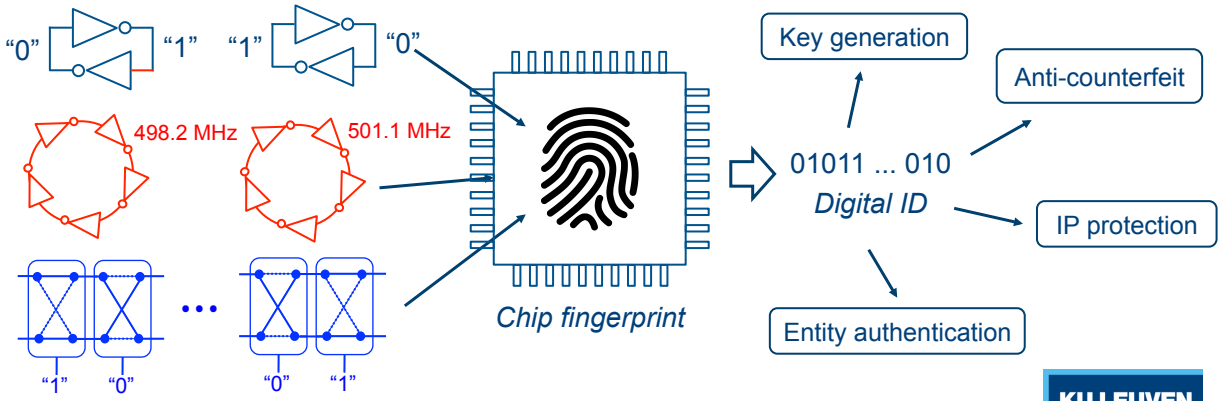
Silicon PUF: An unique fingerprint of a chip

- PUF can be viewed as an *unique* fingerprint of a chip
- Comes from *random process variations*
- Various implementations and applications



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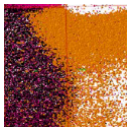
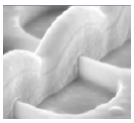
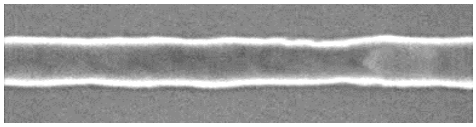
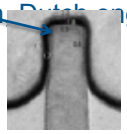
Silicon PUFs - Variability

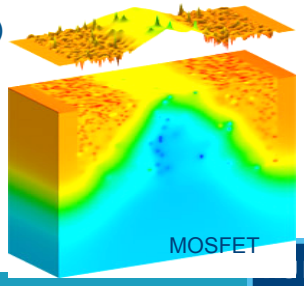


- Silicon Biometrics
- Variability in transistors and interconnect
- In general undesired, except for PUFs
- Random dopant fluctuation
- Tox
- Line edge/width roughness
- Crucial design challenge with CMOS down scaling (Moore's law)
  Pelgrom's law: $\sigma^2 \sim 1/WL$ (Marcel Pelgrom, Dutch engineer)









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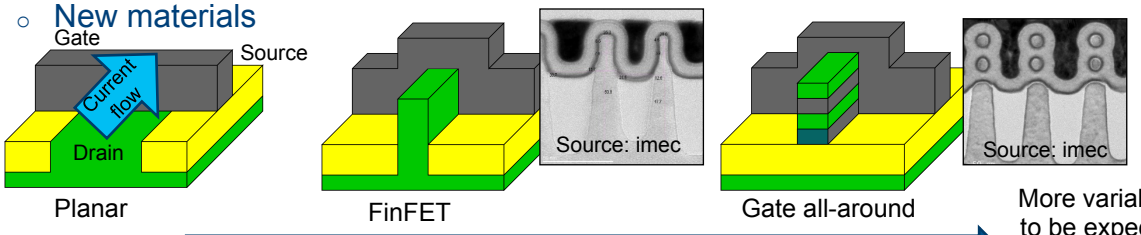
More opportunities brought by scaling

- Even more challenging to manufacture identical devices in scaled technologies
  - Moore's Law
  - 40nm → 28nm →16nm → 7nm → ...
- More variability comes from:
  - More processing steps
  - Decreased size (e.g. 2nm difference → **5%** in 40nm and **30%** in 7nm)
  - New materials



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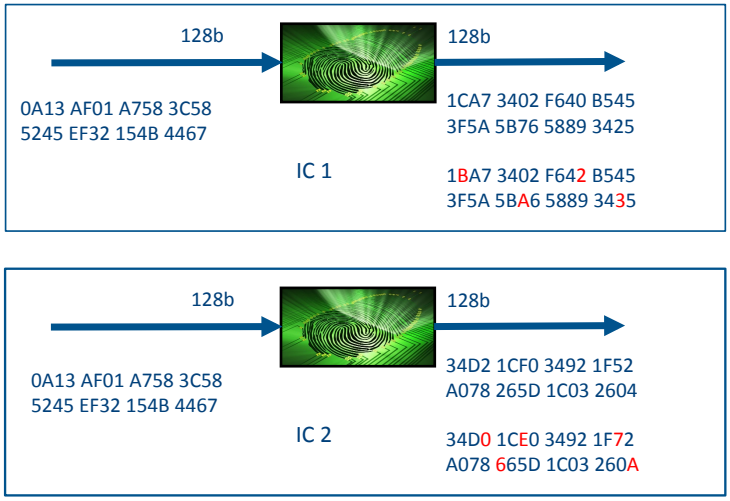
The ideal PUF?



Chip-dependent binary function with noisy output

Evaluation 1

≈ 1-15% noise

Evaluation 2

Evaluation 1

Evaluation 2 ≈ 1-15% noise

IDEAL PUF is without noise

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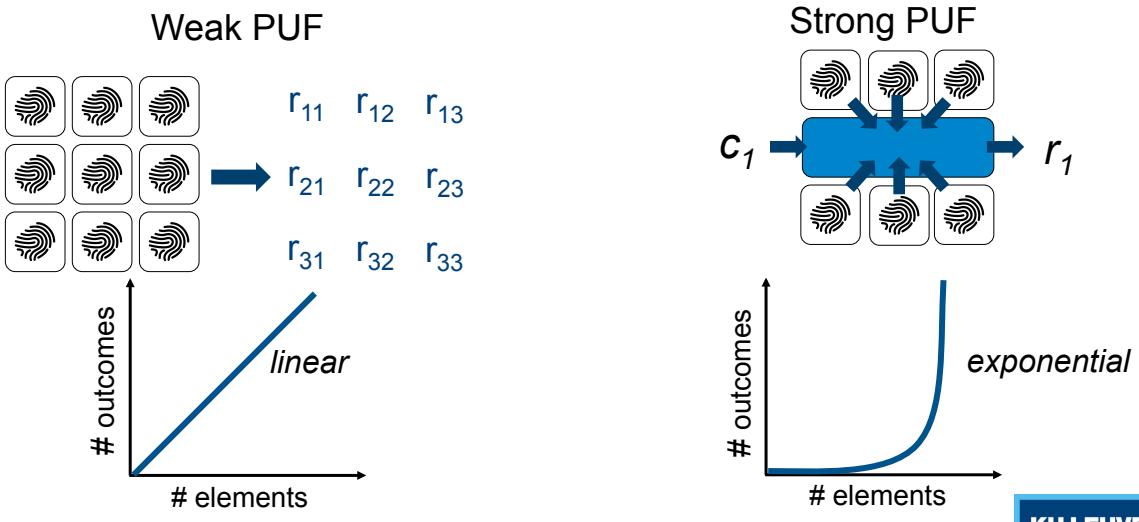
Two design methodologies

Dream 1: IDEAL PUFS don't exist..



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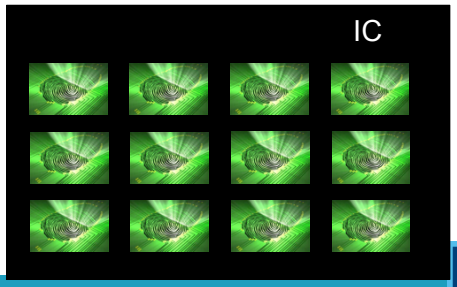
Weak PUF

- An array of identically designed circuit elements
- Each producing 1 (or a few) response bit(s)
- High-quality response bits, i.e., high entropy
- Limited number of bits, e.g., a few 1000s
- Weak because of limited response size, but the best in reality
- E.g., SRAM PUF, spot-break-down PUF
- Typical application: key generation

  E.g. 128-bit AES



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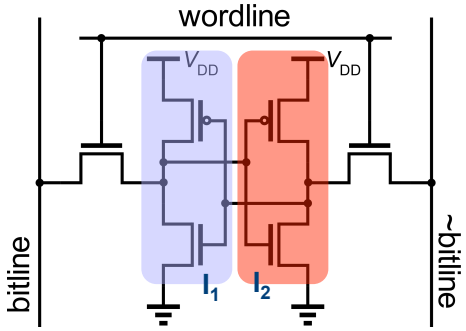
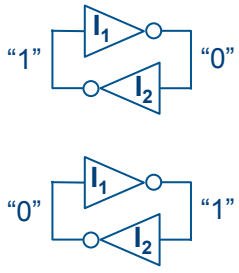
SRAM PUF – a classic weak PUF

- 2D array of 1-bit memory cells
- Variability: ***mismatch*** between the cross-coupled inverters
- Volatile: data is cleared after power-off



6T-SRAM cell



Bi-stable states

Two possible outcomes after power-up

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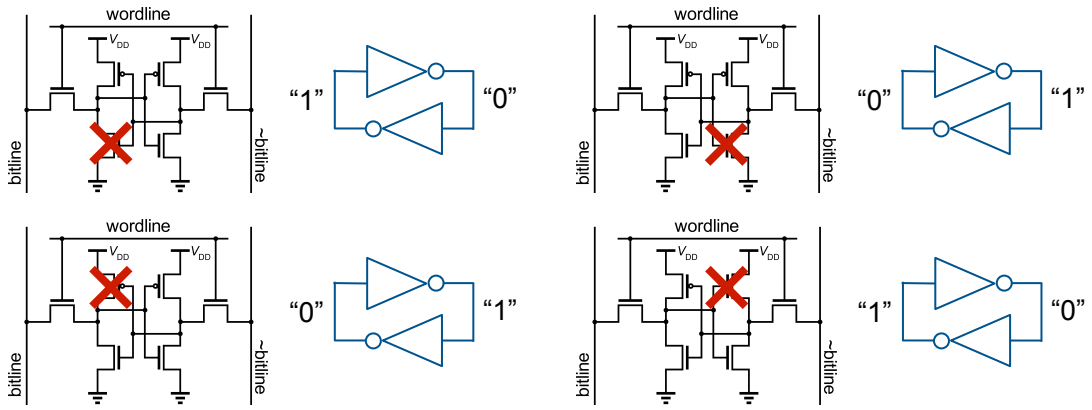
Transistor variations determines PUF bits

- Assume one of the transistors is much weaker than others
- Four extreme cases



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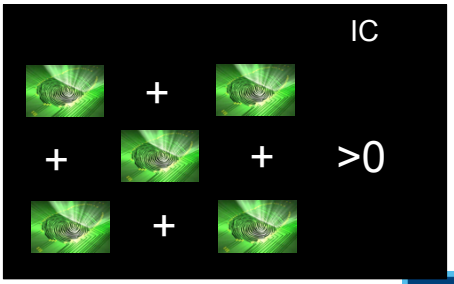
Strong PUF

- Finite number of physical building blocks combined with mathematical operations
- E.g., sum of delays, currents, voltages etc.
- Can produce a gazillion of response bits (2^{128}) ➔ Strong
- Low-quality bits: highly correlated, low-entropy

- E.g., arbiter PUF
- Typical application: IC authentication



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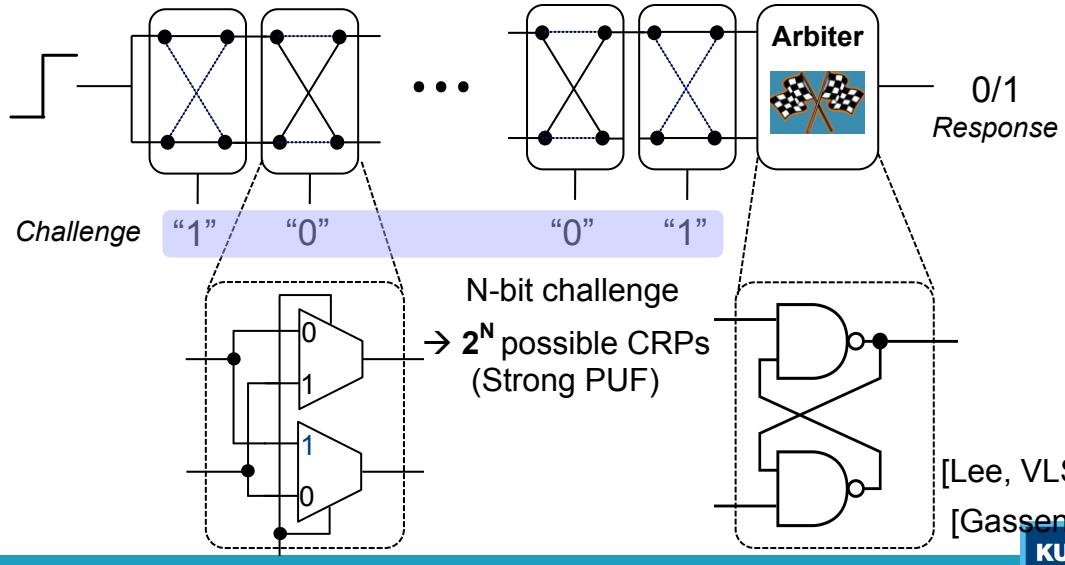
Arbiter PUF – based on timing differences



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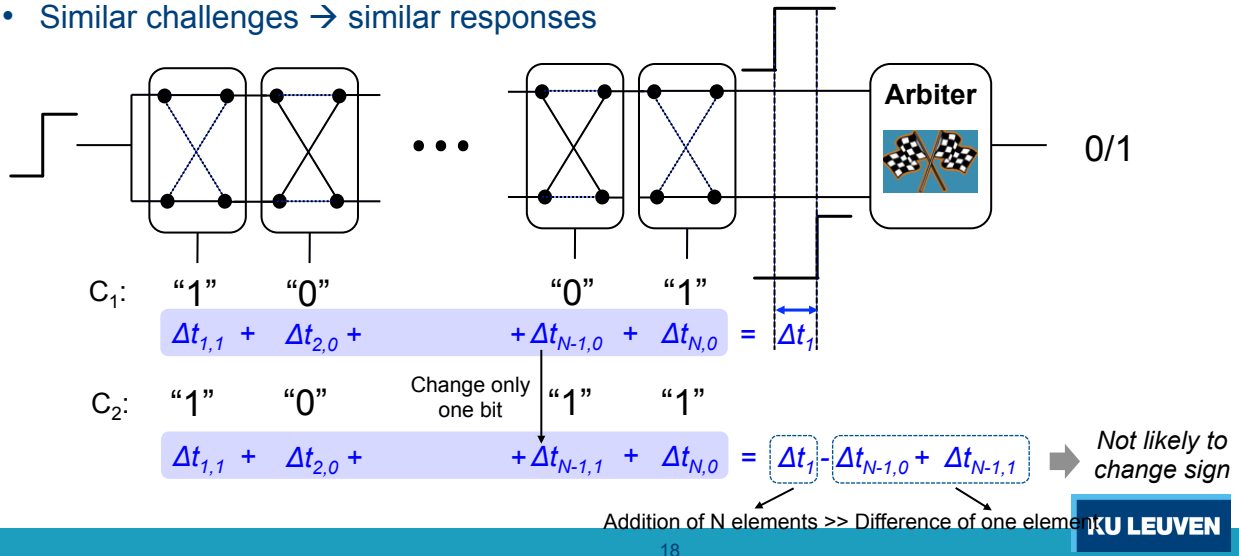
Arbiter PUF is not an ideal strong PUF

- *Linear* additive structure: sum of delays
- Similar challenges → similar responses



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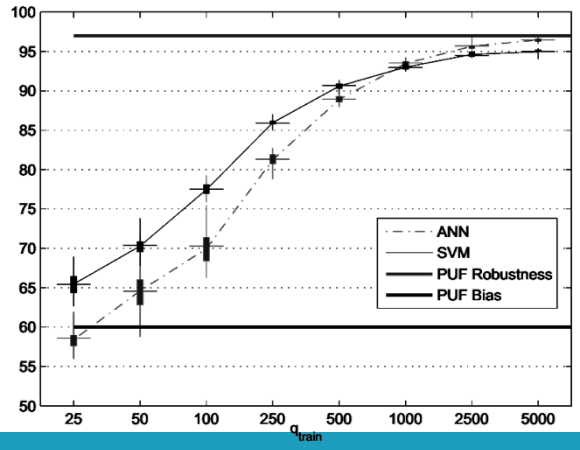
Strong PUF problem: responses easily predicted

- CRPs are highly correlated: low entropy

→ Prone to machine learning (ML) attacks



Experimental results on 65 nm CMOS: only a few 1000 CRPs are sufficient to model the PUF with high accuracy

[Hospodar, WIFS 2012]

[Ruhrmair, ACM CCS 2010]

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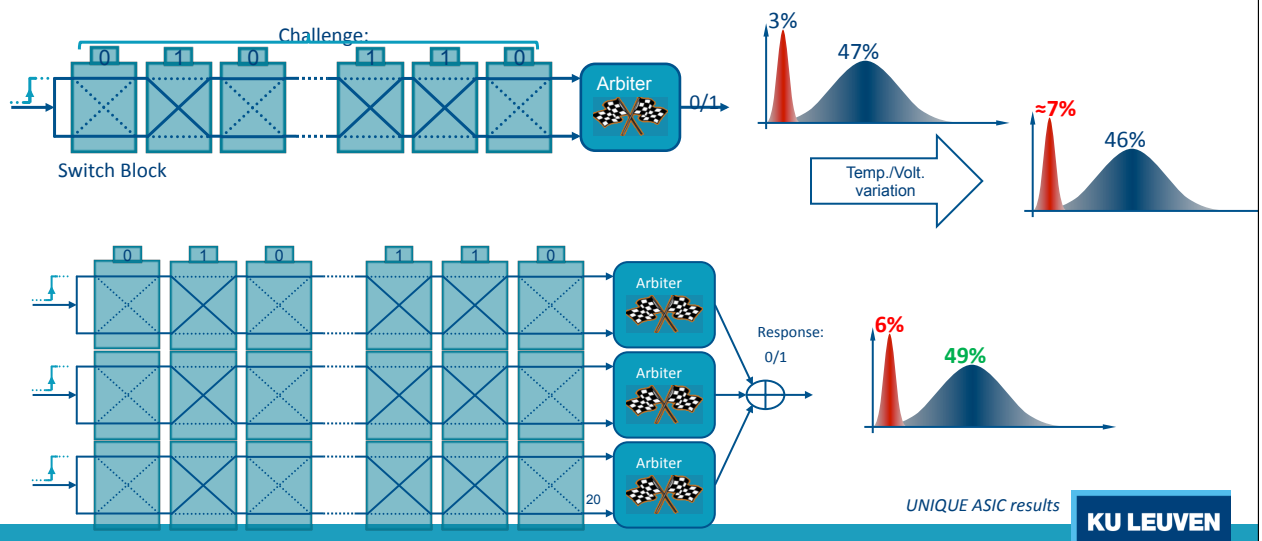
Arbiter PUFs: XOR Variant

- Arbiter PUF: original MIT work
- UNIQUE project result



UNIQUE ASIC results

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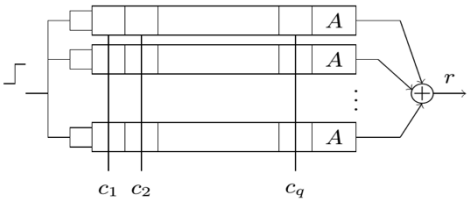
Arbiter PUF – XOR Variant

- XOR the response of multiple chains
- More resistant against machine learning
  - # CRPs in training set ↑
  - Training time ↑
- Unfortunately, noise amplification as well
- Example: Becker et al. at CHES 2015



ML Method	CRP Source	Pred. Rate	No. of XORs	CRPs ($\times 10^3$)	Training Time
LR	FPGA	> 99%	3	19.5	51.5 sec
			4	39	139 sec
			5	78	39 min
LR	ASIC	> 99%	3	19.5	26 sec
			4	39	63.5 sec
			5	78	18:09 min

[Ruhrmair, IEEE TIFS 2013]

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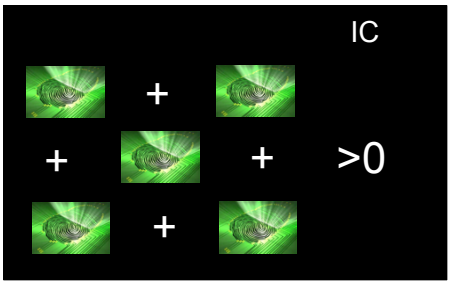
Dream or future research?



Wish a strong PUF:

- Finite number of elements
- Gazillion Challenge Response Pairs
- Non-linear combination to resist modeling attacks: ideally cryptographic functions
- BUT: noise amplification makes output not useful

Dream: strong PUF from finite number of elements, resistant to modeling, noise tolerant

Maybe: computational security?

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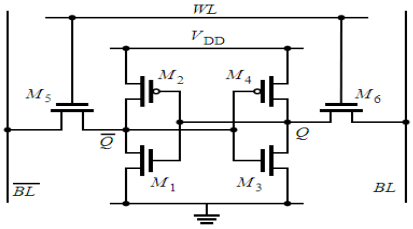
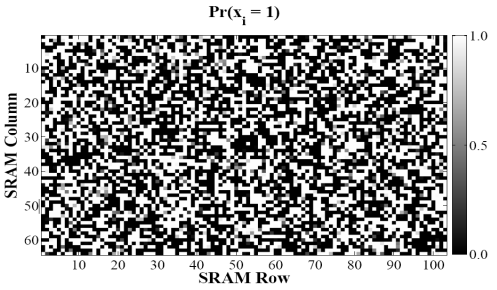
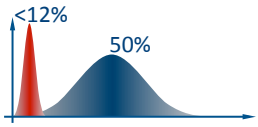
Weak SRAM PUF: Basics

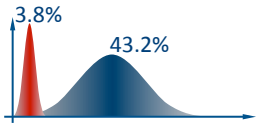


6T CMOS SRAM Cell

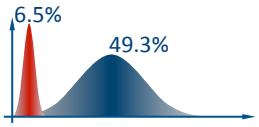




Guajardo et al. 2007, FPGA SRAM temp./volt. var.



Holcomb et al. 2009, Commercial SRAM



Holcomb et al. 2007, Embedded SRAM

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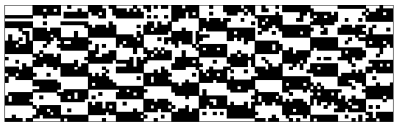
PUF behavior of SRAM in commodity micro-controller

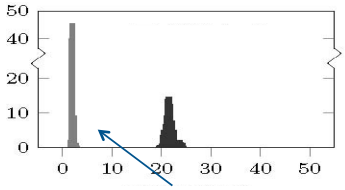
Black box approach (off the shelf micro-controllers)

- PIC16F1825

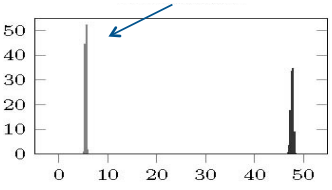


- STM32F100R8

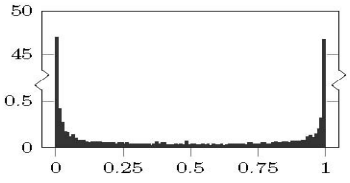
Within and between class HD (%)

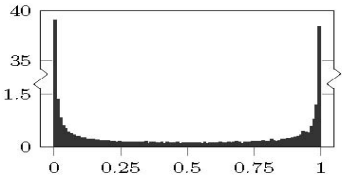


Within Class



Average bit value (%)





[PhD Anthony VH]

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Black box approach (off the shelf micro-controllers)

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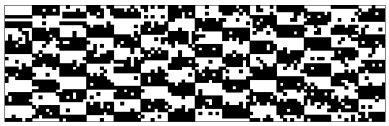
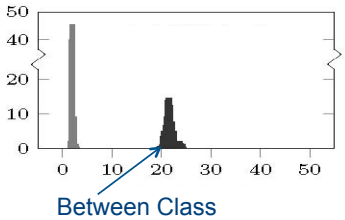
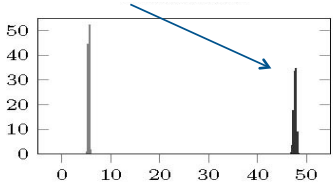


- STM32F100R8

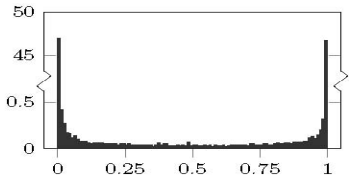
Within and between class HD (%)

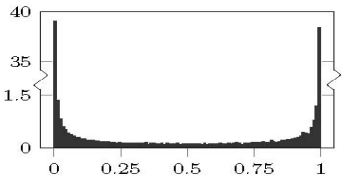


Between Class



Average bit value (%)





Needs post-processing to create key!

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Reliability

- PUF responses are not exactly reproducible
  - At different time
  - In different environment

PUF response r_1=

#1: 101001001010100 01...

#2: 1011010100**0**01010001...

#3: 1010011**1**0101010001...

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Short-term reliability (data stability)

- PUF response changed temporarily caused by:
  - Environment change (external)
  - Internal fluctuation

External:
- Temperature
- Supply voltage
- Humidity
- Radiation
- ...

Internal
- White noise
- Flicker noise
- Cross-talk
- Glitch
- ...

How to improve the short-term reliability?

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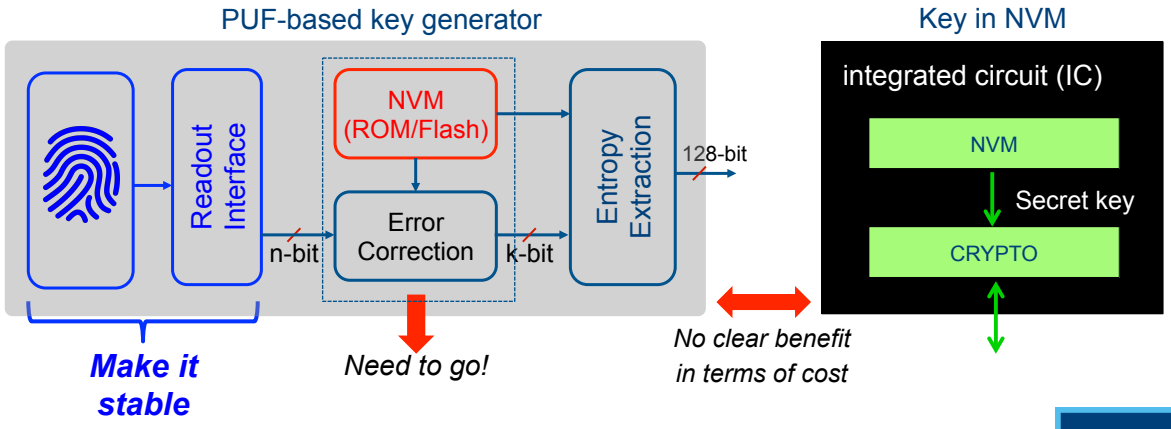
Good reliability is crucial

- Error correction codes need to be stored → NVM needed
- Why not just store the key in NVM?



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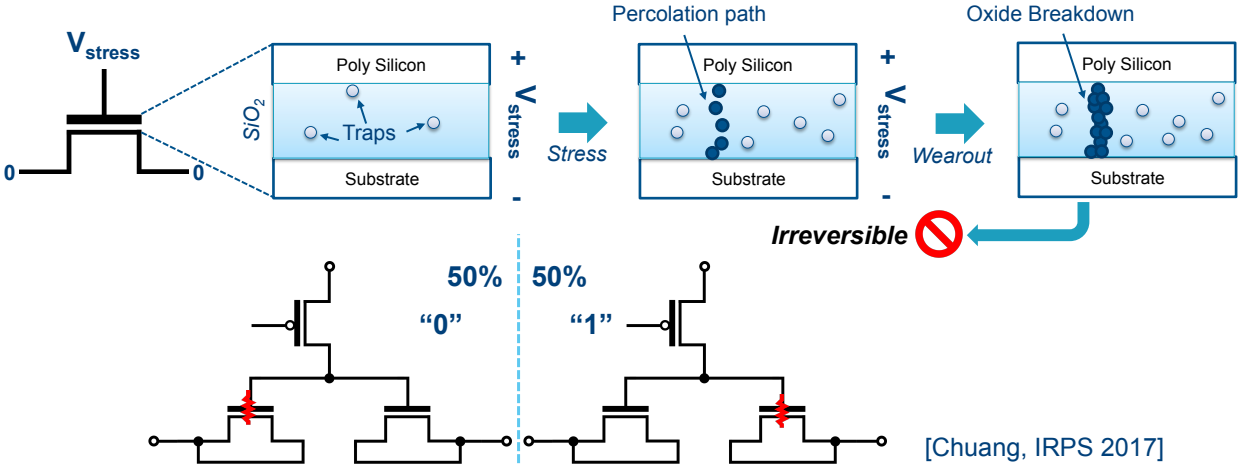
Oxide breakdown spots are natively stable



[Chuang, IRPS 2017]

Time dependent dielectric breakdown (TDDB) can be accelerated by voltage → Less time consuming

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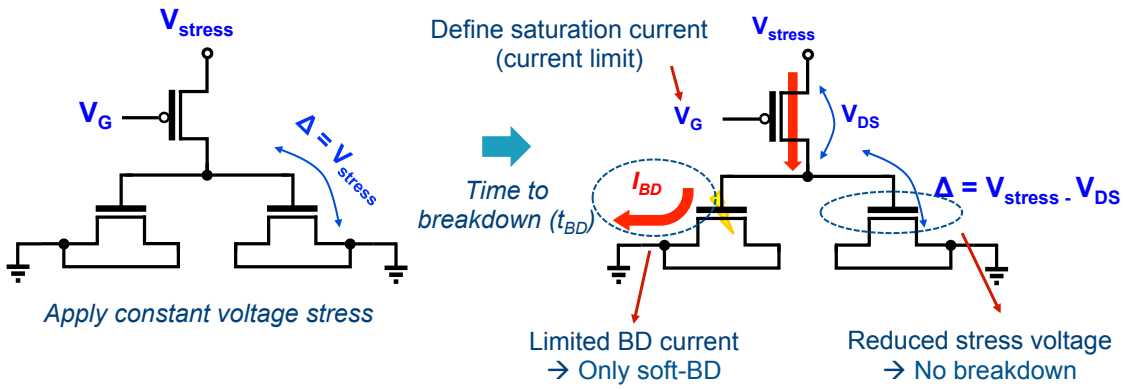
Generating only one BD spot



- Current and voltage are limited by the PMOS selector
- Multiple BD spots are unlikely to happen

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Spot breakdown PUF circuits

imec

IMEC Breakdown PUF [patent]

Random Spatial Distribution

Si proven stable PUF

- ✔ Low cost, low power for IoT, reliable, small footprint
- ✔ Both random key generation & programmable keys

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PUF Usage

Strong PUF: Entity authentication

Weak PUF: Key Generation

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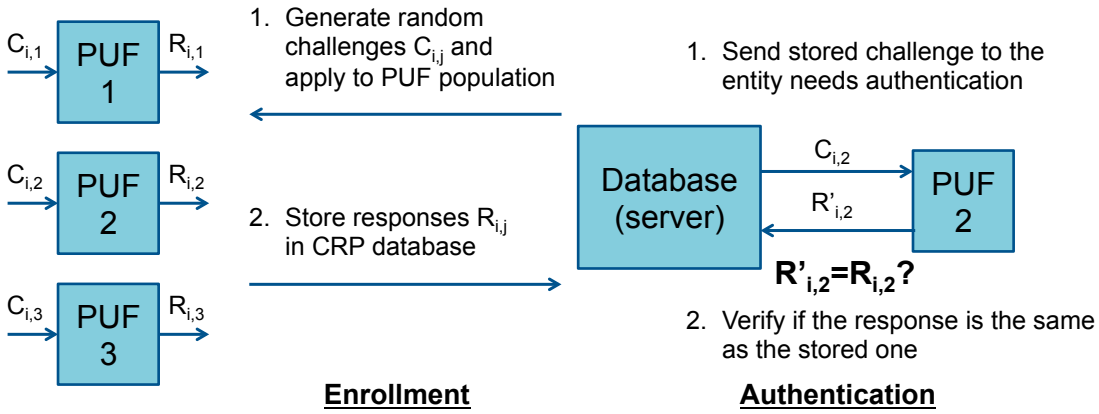
Realizing an ideal authentication scheme

- Entity authentication based on challenge and response



*Needs a huge amount of **uncorrelated** challenge-response pairs (CRPs)*

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Protocols for strong PUFs

A large-scale study of strong PUF protocols:

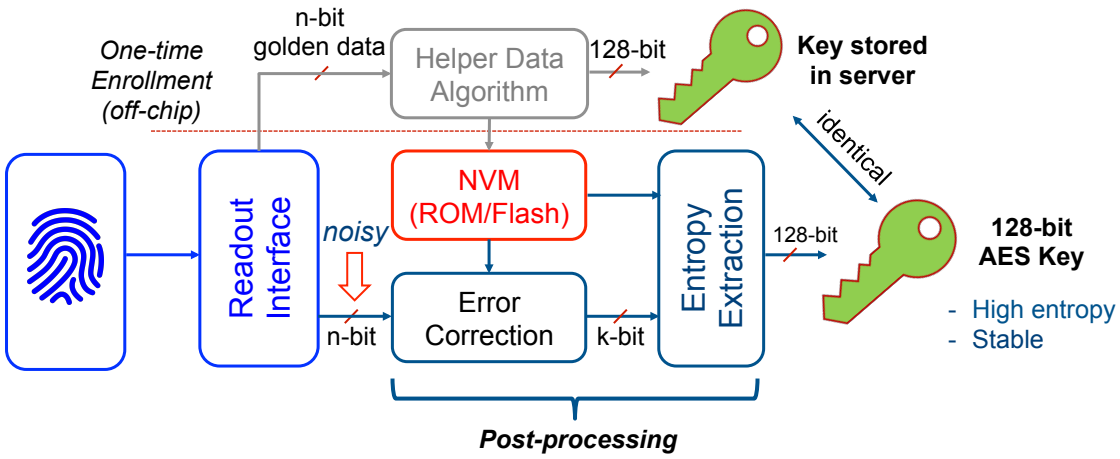
„Secure Lightweight Entity Authentication with Strong PUFs: Mission Impossible?“

[Delvaux, CHES 2014]

[Delvaux, ACM Comp. Surveys 2015]

		Reference II-A	Reference II-B	Basic	Controlled	Bolotnyy et al.	Öztürk et al.	Hammouri et al.	Kulseng et al.	Sadeghi et al.	Reconfiguration	Reverse FE I	Reverse FE II	Converse	Lee et al. I	Jin et al.	Slender	Xu et al.	He et al.	Jung et al.	Lee et al. II	Noise bifurcation	System of PUFs
resources (#6)	Weak PUF	✓	✓	×	×	×	×	×	×	×	×	×	✓	×	×	×	×	×	×	×	×	✓	✓
	Strong PUF[1]	×	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	MTP NVM	×	×	×	×	×	✓	×	×	×	×	×	✓	×	×	×	✓	×	×	×	×	×	×
	TRNG	×	✓	×	×	×	×	✓	×	✓	×	×	✓	✓	×	×	✓	×	×	×	✓	×	×
	Gen	×	×	×	×	×	×	×	×	×	×	×	✓	×	×	×	×	×	×	~	×	×	×
	Rep	✓	✓	×	×	×	×	×	×	×	×	×	✓	✓	×	×	×	×	×	×	×	×	×
	Crypto (Enc/Hash/MAC)	✓	✓	×	✓	×	×	×	×	✓	✓	×	✓	✓	✓	×	×	×	×	✓	×	×	×
	PRNG	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×
	$\oplus, =?$	×	✓	×	×	×	✓	✓	✓	×	×	✓	✓	✓	✓	✓	×	✓	✓	✓	✓	×	×
	$1\times$ interface	✓	✓	×	✓	×	✓	✓	✓	✓	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	×	×
claims	Server authenticity	×	✓	×	×	×	×	×	✓	×	×	✓	✓	✓	✓	✓	×	✓	✓	✓	✓	✓	×
	Token authenticity	✓	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Token privacy	×	×	×	×	✓	×	×	✓	✓	~	×	×	×	×	~	×	✓	✓	✓	✓	×	×
	Leakage resilience (#2)					×	×		×	✓	~				×	✓		×	✓	✓	✓		
	# Authentications	∞	∞	d	d	d	∞	∞	∞	∞	d	∞	∞	∞	d	∞	∞	d	∞	∞	∞	∞	d
evaluation	Noise Robust (#3)	✓	✓		✓	×	~	×	×	✓		✓	✓		×	×	✓	×		×	×	✓	~
	Modeling Robust (#4)	✓	✓	×	✓	×				✓	×	✓	✓				✓	~				✓	×
	PUF Independency (#7)	✓	✓		~					✓		×	✓				×					×	
	Server authenticity (#8)		✓							~		~	✓	×	✓	×		×	×	×			
	Token authenticity (#8)	✓			✓				×	✓		✓	✓		✓		~		×	×		✓	
	Token privacy (#8)								×	✓									×	×			
	DoS prevention (#8)	✓	✓		✓	×	×		×	✓	×	✓	✓		×	×	✓		×	×	×	✓	
	Leakage resilience (#8)								34	✓									×	×			
	Scalability[2] (#9)	✓	✓	✓	✓					×		✓	✓				✓					✓	

From process variation to a secret key



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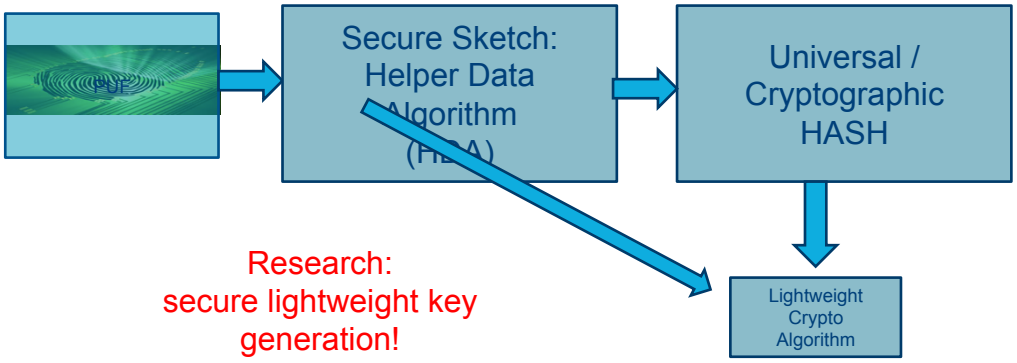
Light weight solution

- PUF is promised as 'light-weight' key generation for Internet of Things, RFID tags, etc.
- Key generation is larger than lightweight algorithm??



Research: secure lightweight key generation!

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True Random Number Generation

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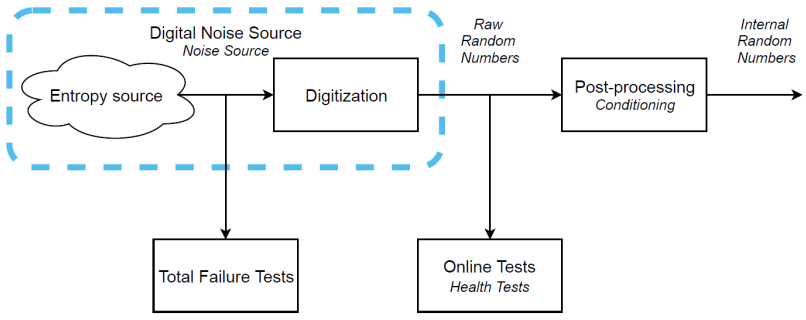
True Random Number Generators



TRNG architecture

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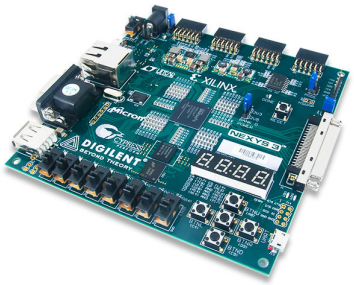
TRNGs on FPGAs



Challenges:

- FPGAs developed to behave in deterministic digital manner
- Vendors' goals: low noise & stable digital behavior → decrease variations of non-deterministic processes → limited number of available noise sources
- TRNG simulations not supported by tools and implementations require special constraints ("set_dont_touch")

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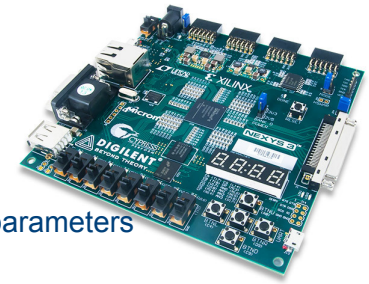
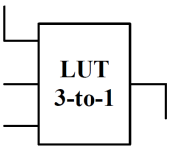
TRNGs on FPGAs

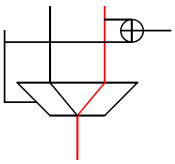


Challenges:

- Portability: different FPGAs → different structure & physical parameters
- Maintain claimed security level on different platforms
- Unrealistic noise assumptions



Fast carry structure on Cyclone IV Intel



Fast carry structure on Spartan 6 Xilinx

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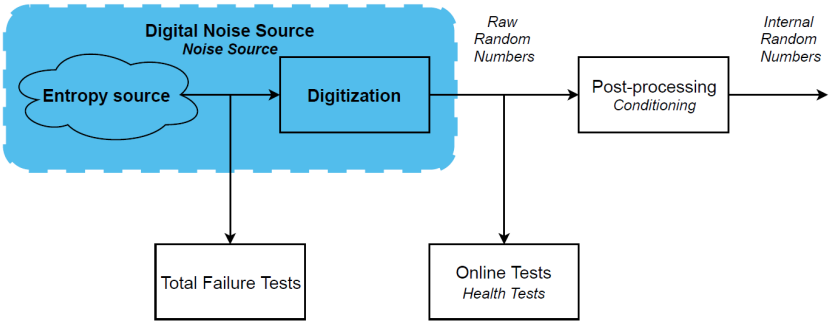
Digital noise sources on FPGAs



TRNG architecture

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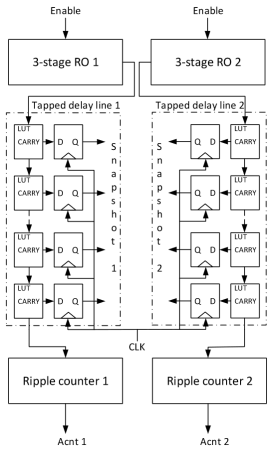
Digital Noise Source

- Reliably measuring parameters of randomness generating process
- Sources of randomness:
  metastability & timing jitter
- Solution: on-chip differential jitter measurement
- Isolate contribution of the white noise:
  - differential setup → reduce global noise
  - short measurement time → reduce flicker noise
- Lower bound on jitter strength → conservative entropy estimate



Intel Cyclone IV

[Yang et al., AsianHOST'17]

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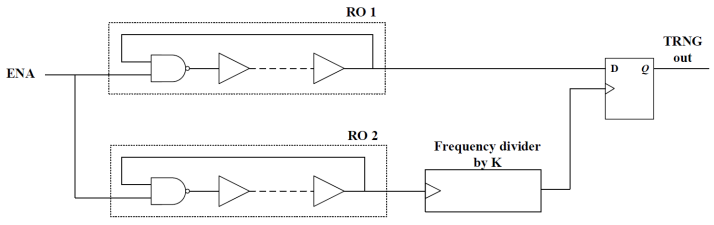
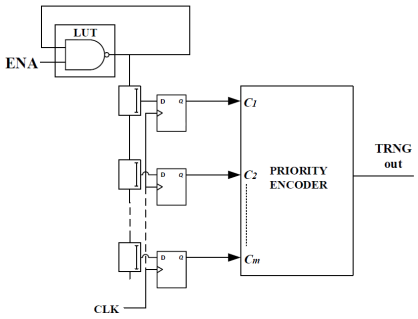
Architectures suitable for FPGAs

- Entropy source: timing jitter
- Time deviation from a periodic signal due to random noise - accumulates *very slowly*
- Relatively easy to model
- Susceptible to temperature and voltage variations



Elementary oscillator based TRNG [BLMT11]



Delay chain TRNG [Rožić et al., DAC'15]

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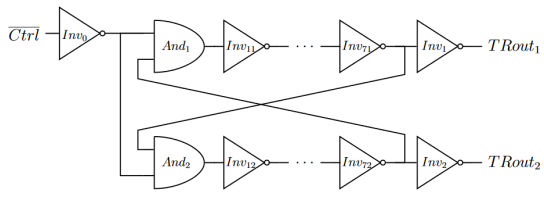
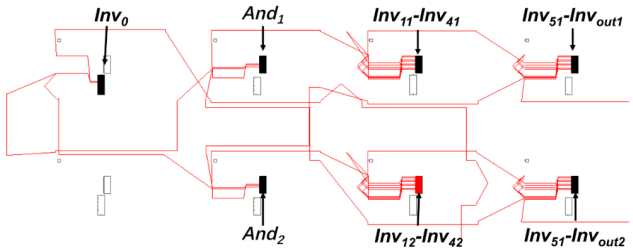
Architectures suitable for FPGAs

- Transition Effect Ring Oscillator (TERO) TRNG
- entropy source: oscillator metastability
- digitizer: asynchronous counter → LSB used as random bit
- manual placement and routing of LUTs
- high throughput (1.3 Mb/s)



[VD10]



[Cao et al., MWSCAS'16]

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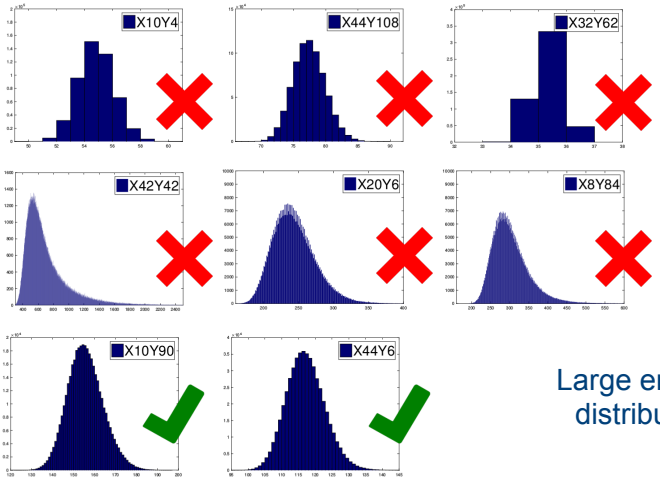
TERO TRNG on FPGAs

- Influence of FPGA location on oscillation occurrence



Very few transitions

Statistical defects

Large enough number of transitions (> 100), distribution close to Gaussian, pass NIST SP800-22

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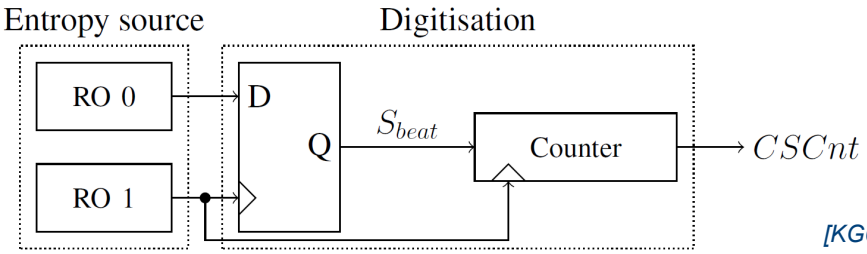
Architectures suitable for FPGAs

- ➢ Coherent Sampling (COSO) TRNG
- entropy source: timing jitter
- low frequency beat signal S_{beat}
- count period *CSCnt* → LSB is random due to jitter in ROs



[KG04]

✓ High throughput (> 1 Mb/s)

✓ Low area

✗ Extremely large design effort to match frequencies of the ROs

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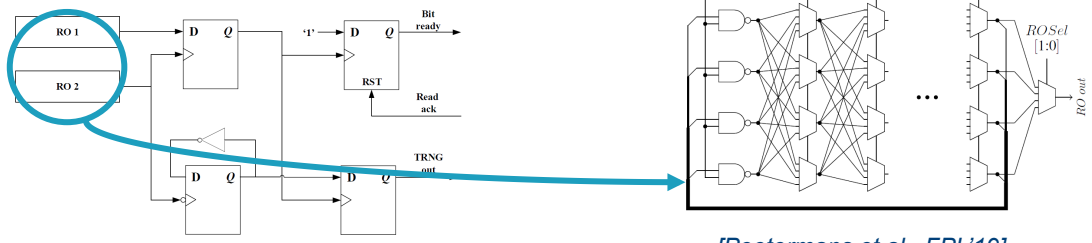
Configurable COSO TRNG

- Reconfigurable ROs
- Controller with dynamic calibration



[Peetermans et al., FPL'19]

- ✓ 'Plug & Play' solution → no manual P&R
- ✓ Low design effort and high portability
- ✓ High throughput: 3.3 Mb/s on *Spartan 6* & 1.5 Mb/s on *SmartFusion 2*
- – Price paid: increased latency

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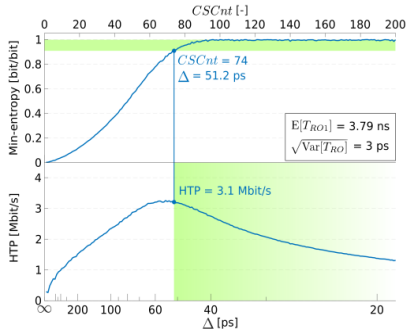
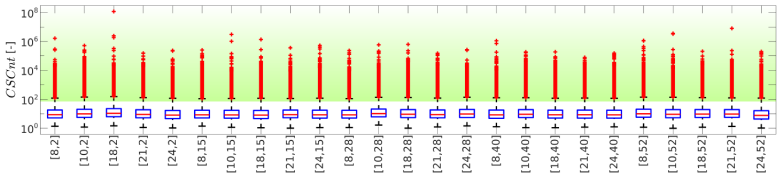
Configurable COSO TRNG - COCOSO





FPGA placement [x,y]

- Find optimal point to obtain both high throughput and high entropy – HTP (min-entropy throughput product)
- Sufficient matching of RO frequencies obtained for all FPGA locations

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Configurable COSO TRNG – Implementation results

Architecture	FPGA family	Area [DFF/LUTs]	Throughput [Mb/s]	Statistical tests	Design effort
Configurable COSO	*Spartan 6*	39/108	3.3	AIS-31 T6-T8	-
	SmartFusion 2	38/111	1.47	AIS-31 T6-T8	-
Original COSO	*Spartan 6*	3/18	0.54	AIS-31 T8	MP
	SmartFusion 2	3/23	0.328	AIS-31 T8	MP
TERO TRNG	*Spartan 6*	12/39	0.625	AIS-31 T8	MP & MR
	SmartFusion 2	12/46	1	AIS-31 T8	MP & MR
STRNG	*Spartan 6*	256/346	154	AIS-31 T8	MP & MR
	SmartFusion 2	256/350	188	AIS-31 T8	MP & MR

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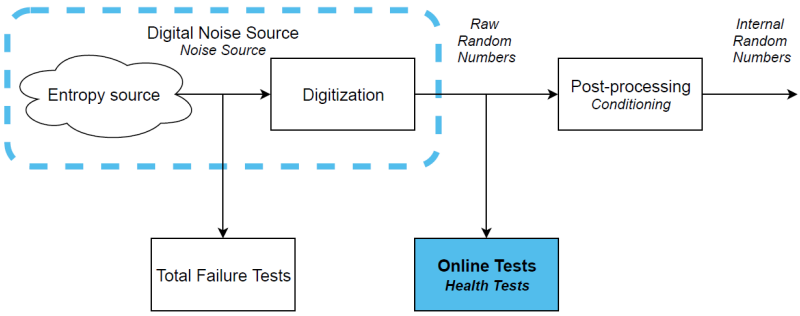
Online tests



TRNG architecture

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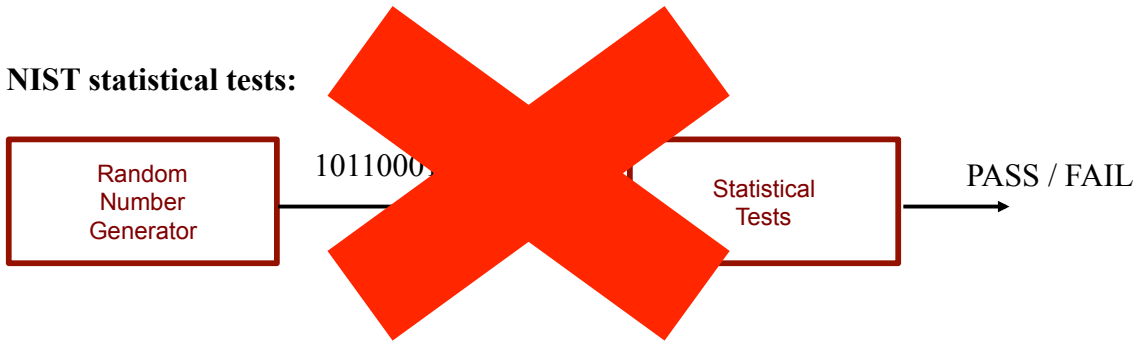
TRNG: the old school



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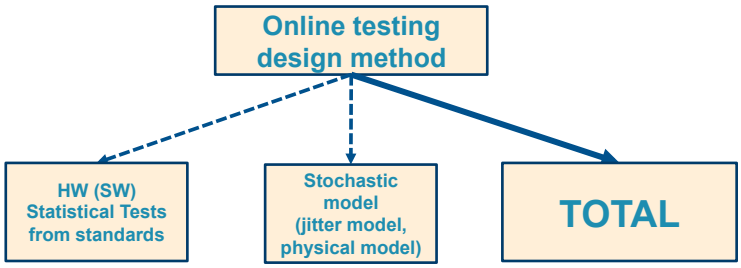
Online tests: TOTAL methodology



[Yang et al., DATE'16]

TRNG On-the-fly Testing for Attack Detection using Lightweight Hardware

- Experiment oriented design methodology
- Tests tailored for entropy source and attacks

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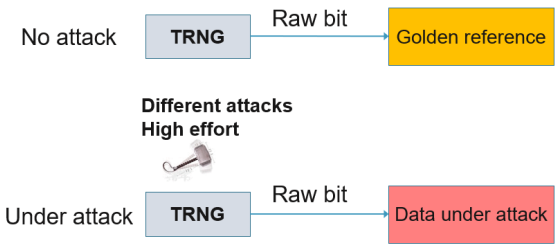
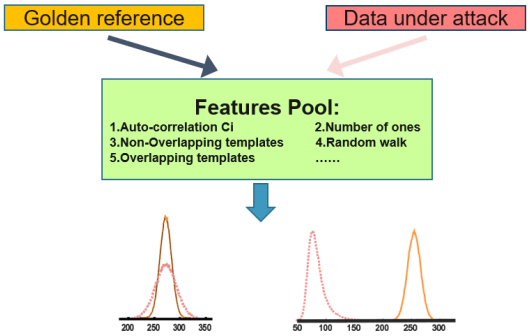
Online tests: TOTAL methodology

- Step 1: Data collection



- Step 2: Selection of useful features



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Online tests: TOTAL methodology

- Step 3: Feature verification

➢ Collect more data to verify the bounds
➢ Test the robustness of the selected features

- Step 4: Attack impact analysis

➢ Check the usefulness under different attack efforts

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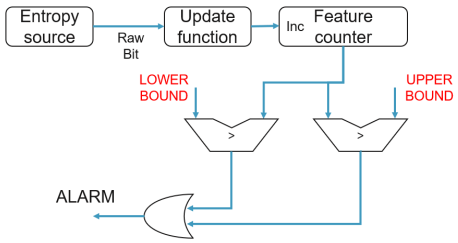
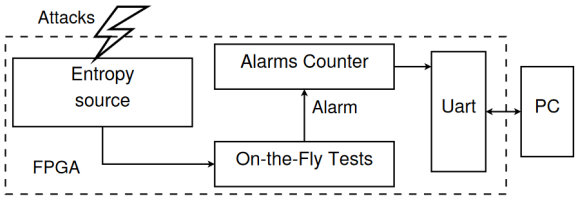
Online tests: TOTAL methodology

- Step 5: HW implementation



- Step 6: HW verification



	Spartan 6 FPGA		
	Slices	LUTs	FFs
Sensitive test	9	28	25
Robust test	10	26	22
Combined test	14	42	35

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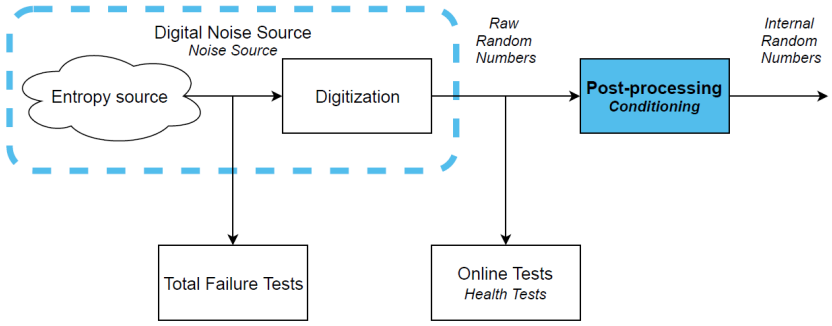
Post-processing



TRNG architecture

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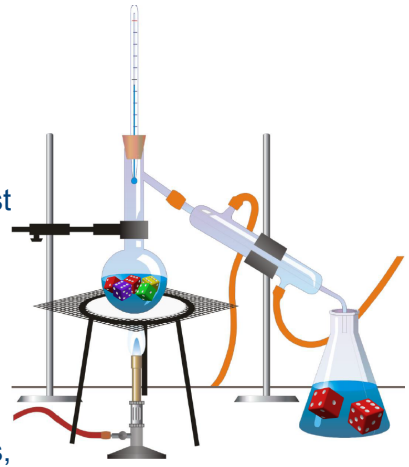
Post-processing

- Cryptographic post-processing
  - High implementation costs i.r.t. TRNG
  - Block ciphers & hash functions
  - Required by AIS-31 standard for the highest security level
- Arithmetic post-processing
  - Low implementation costs
  - Low latency
  - XOR, Von-Neumann debiasing, linear codes, strong blenders



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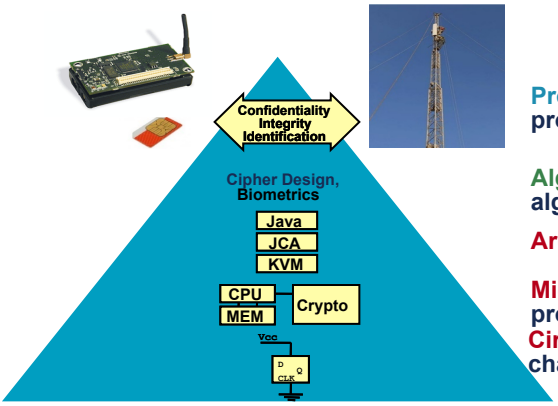
Conclusion: Root of trust: one level down!



Protocol: low power authentication protocol design

Algorithm: public key, secret key, hash algorithms, post-quantum

Architecture: Co-design, HW/SW, SOC

Micro-Architecture: arithmetic, co-processor design

Circuit: Circuit techniques to combat side channel analysis, TRNG's PUFs,

At the bottom: PUFs and TRNGs

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